# Lab 5.1,5.2 NMOS/PMOS I-V Characteristics

This lab plots the set of characteristic curves for the MosFets (we do not have the dual matched Motorola ICs named in the lab descriptions so use the small signal MosFets that we have) that will be used in the next two experiments. Once again, you can be smarter about getting your data in both the simulator and in the actual circuits and get data in without taking the readings one at a time as I suggested in the Diode I-V experiment earlier. If your team runs short of time, it is sufficient to simulate both MosFets, but only measure one of them. Be sure to get estimates of threshold voltages and transconductance of your MosFet since they will be significantly different (look up the on-line descriptions of your MosFets and the Motorola ICs) from the Motorola ICs that the lab descriptions assume. Download and reference the specification sheet for the MosFet you are using.

The "N" or "P" in the name describes the majority carrier in the MosFet "channel" (current flows between the "Drain" and the "Source" through the channel). The "MOS" stands for Metal-Oxide-Semiconductor where the metal "Gate" is insulated from the channel by a layer of SiO_2 (glass).
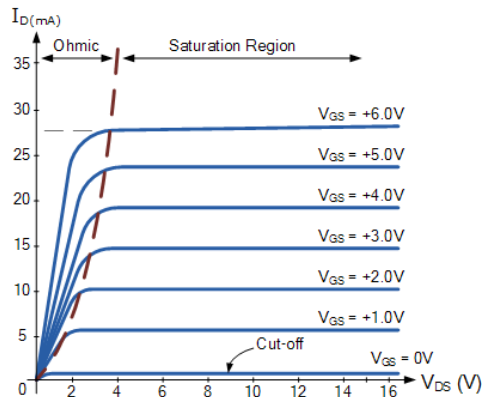
Your NMOS enhancement mode characteristic curves should look something like the graph on the left, but with different parameters

- Your "threshold voltage" will not be 0
- Your "Transconductance" (I_D/V_{GS}) may be very high, so don't overheat your MosFet (use small V_{GS} steps).

The polarities will be reversed for a PMOS device.

Warning: the PMOS symbol in Multisim is very confusing in all cases choose a MOS variant that explicitly shows a "Protection" Drain/Source diode that should always be reverse biased.

There is more about the structure and uses of a MosFet is in the next 2 experiments (5.5, 5.12) description.

Again, the PDFs included here relate to an earlier edition of your text so the chapter numbers, reference pages and figure numbers will not match those in your text.

NMOS I-V Characteristics
(See Sections 5.1–5.2, p. 238 of Sedra/Smith)

OBJECTIVES:

To study NMOS transistor I-V curves by:

- Simulating a transistor to investigate the drain current vs. gate-to-source voltage and drain-to-source voltage.
- Implementing a circuit and taking measurements of the I_D vs. V_{GS} and I_D vs. V_{DS} curves.
- Extracting values of k_n, V_{tn}, and λ_n.

MATERIALS:

- Laboratory setup, including breadboard
- 1 enhancement-type NMOS transistor (e.g., MC14007)
- Several wires
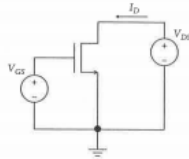
PART 1: SIMULATION

FIGURE L5.1: Transistor measurement circuit.

Consider the circuit in Figure L5.1. Enter the circuit into your simulator's schematic editor, applying DC voltage supplies to the gate and drain of the transistor.

PMOS I-V Characteristics
(See Sections 5.1–5.2, p. 232 of Sedra/Smith)

OBJECTIVES:

To study PMOS transistor I-V curves by:

- Simulating a transistor to investigate the drain current vs. gate-to-source voltage and drain-to-source voltage.
- Implementing a circuit and taking measurements of the I_D vs. V_{SG} and I_D vs. V_{SD} curves.
- Extracting values of k_p, V_{tp}, and λ_p.

MATERIALS:

- Laboratory setup, including breadboard
- 1 enhancement-type PMOS transistor (e.g., MC14007)
- Several wires
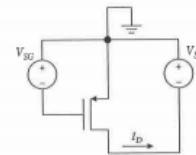
PART 1: SIMULATION

FIGURE L5.2: Transistor measurement circuit.

Consider the circuit in Figure L5.2. Enter the circuit into your simulator's schematic editor, applying DC voltage supplies to the gate and drain of the transistor. In the diagram, the source is indicated as the reference node (ground). What voltages would you need to apply if another node, e.g., the drain, were labeled as the reference?

I_D vs. V_{GS}

While setting V_{DS} to a constant value of 5 V, sweep the gate voltage from 0 V to 5 V in increments of 0.1 V. Plot a curve of I_D vs. V_{GS}. At what value of V_{GS} does the current turn on?

I_D vs. V_{DS}

For three values of V_{GS} (2.5 V, 3.0 V, and 3.5 V), sweep the drain voltage from 0 V to 5 V in increments of 0.1 V. Plot the curves for I_D vs. V_{DS} onto a single graph, clearly indicating the value of V_{GS} next to each curve.

PART 2: MEASUREMENTS

Assemble the circuit from Figure L5.1, using a power supply to generate the DC voltages.

I_D vs. V_{GS}

While setting V_{DS} to a constant value of 5 V, sweep the gate voltage from 1.0 V to 3.5 V in increments of 0.25 V (note, we have reduced the number of data points with respect to the simulations), and measure the drain current using the power supply. (*Note:* Not all power supplies allow you to measure current accurately; if this is the case for your lab setup, you may place a small resistor in series with the drain and measure the voltage drop across the resistor.) Plot a curve of I_D vs. V_{GS}. At what value of V_{GS} does the NMOS turn on?

I_D vs. V_{DS}

For three values of V_{GS} (2.5 V, 3.0 V, and 3.5 V), sweep the drain voltage from 0 V to 3.5 V in increments of 0.5 V, and measure the drain current using the power supply. Plot the curves for I_D vs. V_{DS} onto a single graph, clearly indicating the value of V_{GS} next to each curve.

PART 3: POST-MEASUREMENT EXERCISE

Simulation vs. measurement

What are the main differences between your simulated and measured curves? Can you explain the differences?

Parameter extraction

(1) Threshold voltage, V_{tn}
From the measured I_D vs. V_{GS} curve, at what value of V_{GS} does the NMOS turn on? Set this as the threshold voltage V_{tn} of your transistor.

(2) MOSFET transconductance parameter, k_n
Based on the value of drain current I_D at V_{GS} = 3.0 V, and using the saturation model for the transistor, i.e., $I_D = (1/2)k_n(V_{GS} - V_{tn})^2$, extract the value of $k_n = \mu_n C_{ox}(W/L)$. Using your extracted values of V_{tn} and k_n, plot a curve of I_D vs. V_{GS},

using the saturation model, and compare with your simulated and measured curves. Are there any differences? Can you explain the differences?

(3) Early voltage, V_A
Based on your measured I_D vs. V_{DS} curves for a saturated transistor, extract the Early voltage V_A. Does V_A change significantly for each value of V_{GS}? What is the average value of V_A? Based on your average value of V_A, calculate $\lambda_n = 1/V_A$.
Repeat Steps 1 to 3 for your measured results.
Summarize your results in the following table.

	MEASURED
V_{tn} [V]	
k_n [mA/V²]	
λ_n [V⁻¹]	

PART 4 [OPTIONAL]: EXTRA EXPLORATION

If you have access to a semiconductor parameter analyzer, generate the I_D vs. V_{DS} curves using the analyzer. How do they compare to the curves you generated in Part 3? Re-extract values of V_{tn}, k_n, and λ_n.

I_D vs. V_{SG}

While setting V_{SD} to a constant value of 5 V, sweep the gate voltage from 0 V to –5 V in increments of 0.1 V. Plot a curve of I_D vs. V_{SG}. At what value of V_{SG} does the PMOS turn on?

I_D vs. V_{SD}

For three values of V_{SG} (2.5 V, 3.0 V, and 3.5 V), sweep the drain voltage from 0 V to –5 V in increments of 0.1 V. Plot the curves for I_D vs. V_{SD} onto a single graph, clearly indicating the value of V_{SG} next to each curve.

PART 2: MEASUREMENTS

Assemble the circuit from Figure L5.2, using a power supply to generate the DC voltages. Note the polarities of the voltage sources. You may need to be creative to get the correct polarities! Remember that for a PMOS transistor that is on, V_{SG}, V_{SD}, and I_D will be positive quantities.

I_D vs. V_{SG}

While setting V_{SD} to a constant value of 5 V, sweep the gate voltage from –1.0 V to –3.5 V in increments of 0.25 V (note, we have reduced the number of data points with respect to the simulations), and measure the drain current using the power supply. (*Note:* Not all power supplies allow you to measure current accurately; if this is the case for your lab setup, you may place a small resistor in series with the drain and measure the voltage drop across the resistor.) Plot a curve of I_D vs. V_{SG}. At what value of V_{SG} does the current turn on?

I_D vs. V_{SD}

For three values of V_{SG} (2.5 V, 3.0 V, and 3.5 V), sweep the drain voltage from 0.0 V to –3.5 V in increments of 0.5 V, and measure the drain current using the power supply. Plot the curves for I_D vs. V_{SD} onto a single graph, clearly indicating the value of V_{SG} next to each curve.

PART 3: POST-MEASUREMENT EXERCISE

Simulation vs. measurement

What are the main differences between your simulated and measured curves? Can you explain the differences?

Parameter extraction

(1) Threshold voltage, V_{tp}
From the measured I_D vs. V_{SG} curve, at what value of V_{SG} does the PMOS turn on? Set this as the threshold voltage V_{tp} of your transistor, but express it as a negative number to be consistent with practice.

(2) MOSFET transconductance parameter, k_p
Based on the value of drain current I_D at $V_{SG} = -V_{tp} + 1$ V, and using the saturation model for the transistor, i.e., $I_D = (1/2)k_p(V_{SG} - |V_{tp}|)^2$, extract the value of $k_p = \mu_p C_{ox}(W/L)$. Using your extracted values of V_{tp} and k_p, plot a curve of I_D vs. V_{SG}, using the saturation model, and compare with your simulated and measured curves. Are there any differences? Can you explain the differences?

(3) Early voltage, V_A
Based on your measured I_D vs. V_{SD} curves for a saturated transistor, extract the Early voltage V_A. Does V_A change significantly for each value of V_{SG}? What is the average value of V_A? Based on your average value of V_A, calculate $\lambda_p = 1/V_A$.
Repeat Steps 1 to 3 for your measured results.
Summarize your results in the following table.

	MEASURED
V_{tp} [V]	
k_p [mA/V²]	
λ_p [V⁻¹]	

PART 4 [OPTIONAL]: EXTRA EXPLORATION

If you have access to a semiconductor parameter analyzer, generate the I_D vs. V_{SD} curves using the analyzer. How do they compare to the curves you generated in Part 3? Re-extract values of V_{tp}, k_p, and λ_p.