Inputs		Output
x	y	z
L	L	H
L	H	H
H	L	H
H	H	L

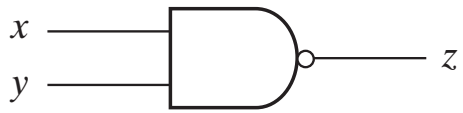


Fig. 10-1 Positive Logic NAND Gate

Inputs		Output
x	y	z
L	L	H
L	H	L
H	L	L
H	H	L

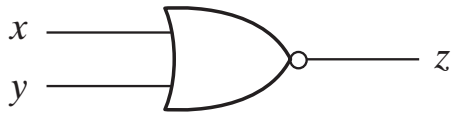
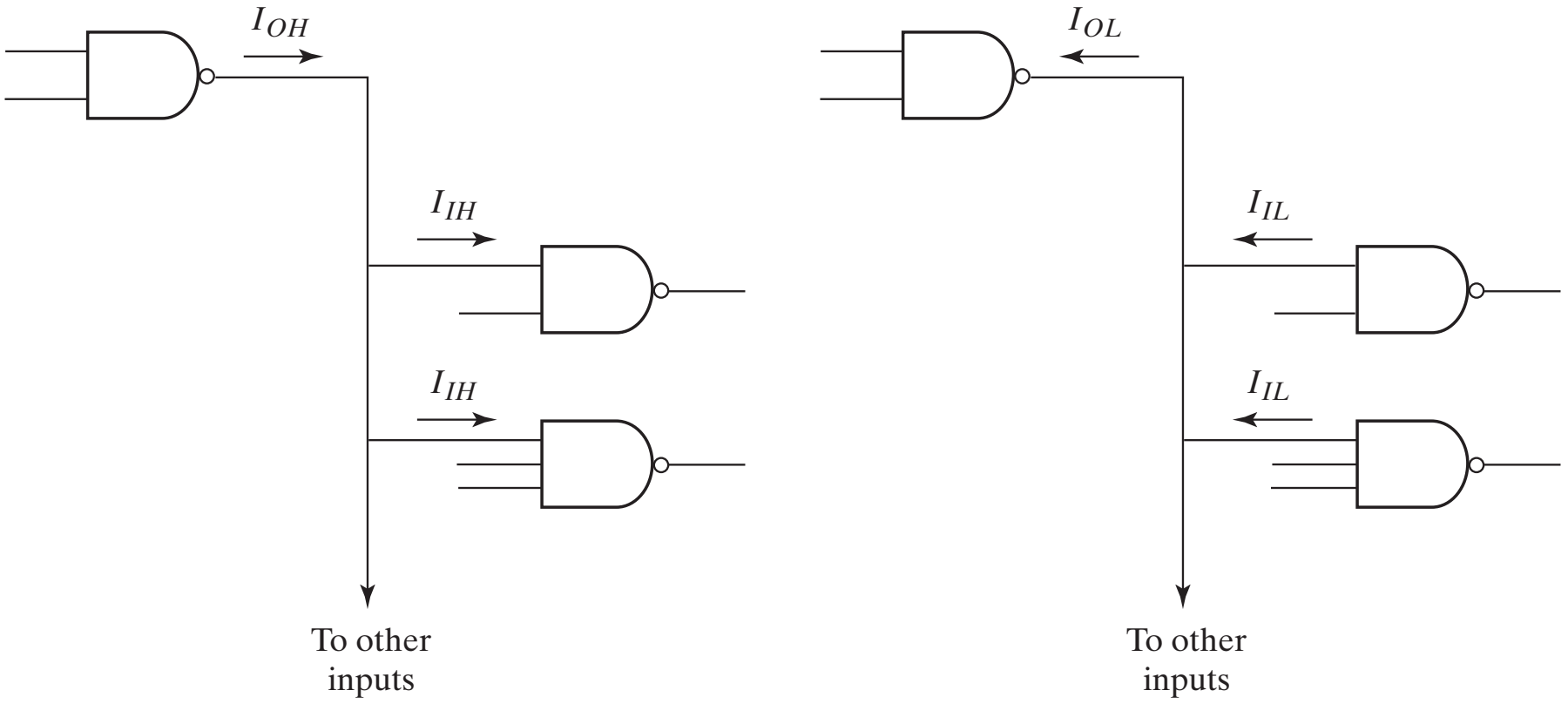


Fig. 10-2 Positive Logic NOR Gate



(a) High-level output

(b)Low-level output

Fig. 10-3 Fan-Out Computation

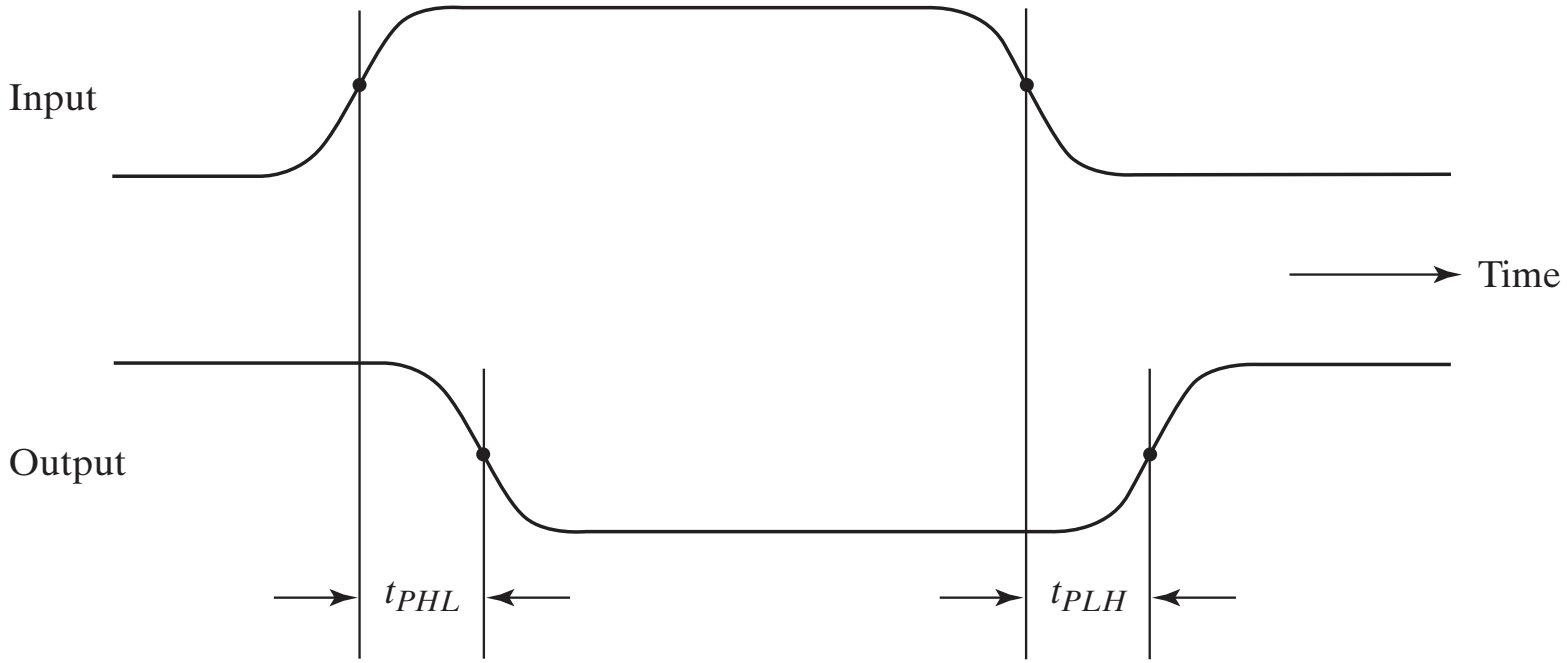


Fig. 10-4 Measurement of Propagation Delay

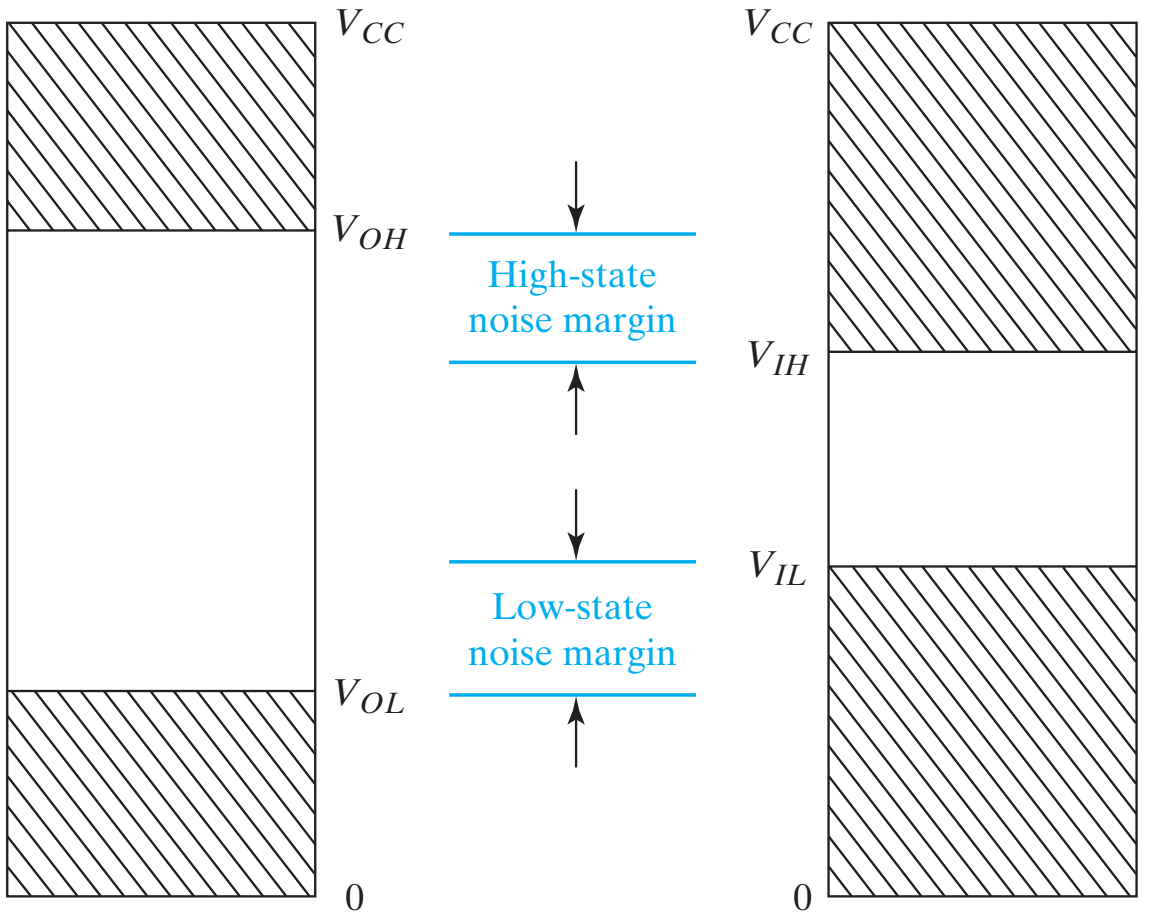
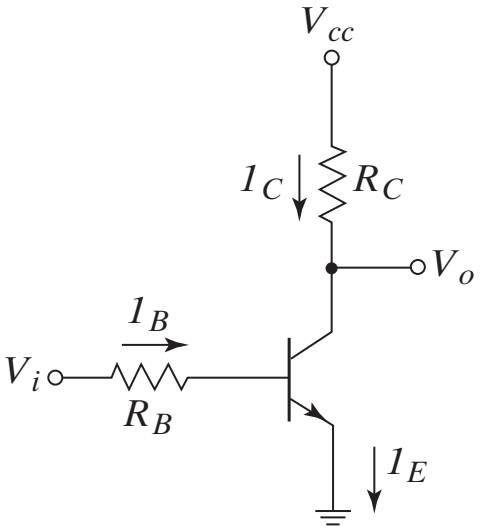
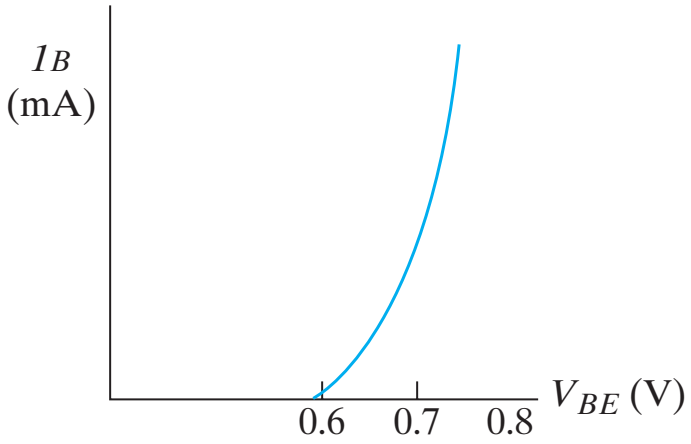


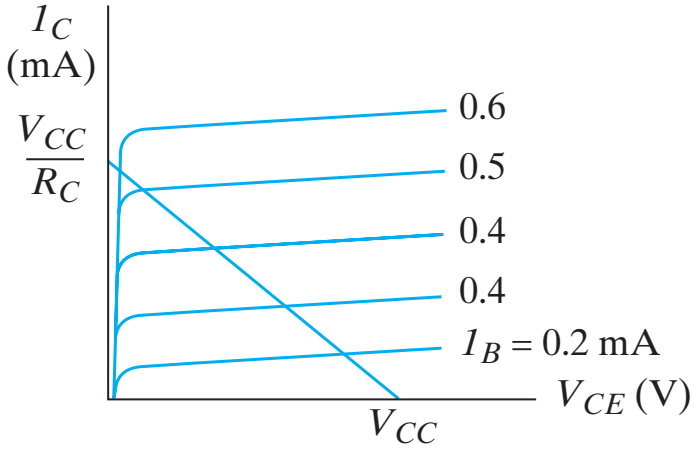
Fig. 10-5 Signals for Evaluating Noise Margin



(a) Inverter circuit

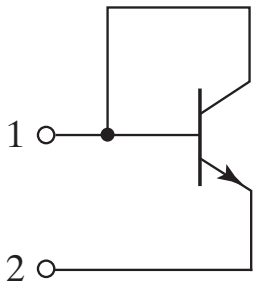


(b) Transistor-base characteristic

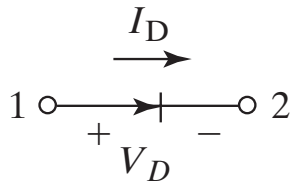


(c) Transistor-collector characteristic

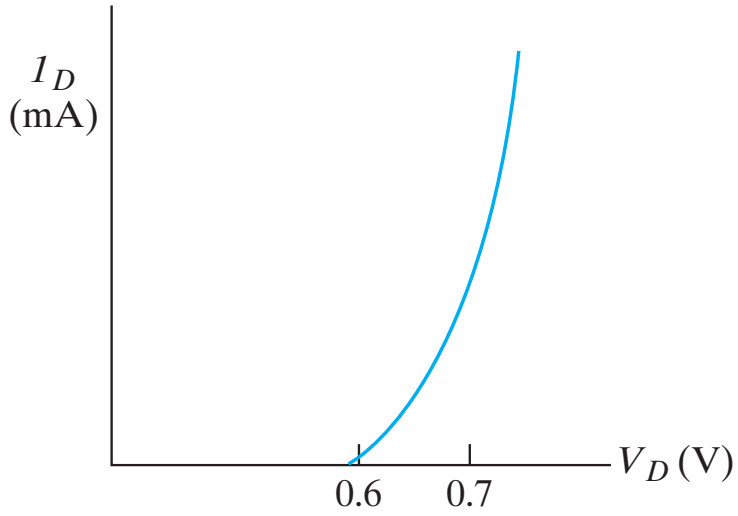
Fig. 10-6 Silicon *npn* Transistor Characteristics



(a) Transistor adapted for use as a diode



(b) Diode graphic symbol



(c) Diode characteristic

Fig. 10-7 Silicon Diode Symbol and Characteristic

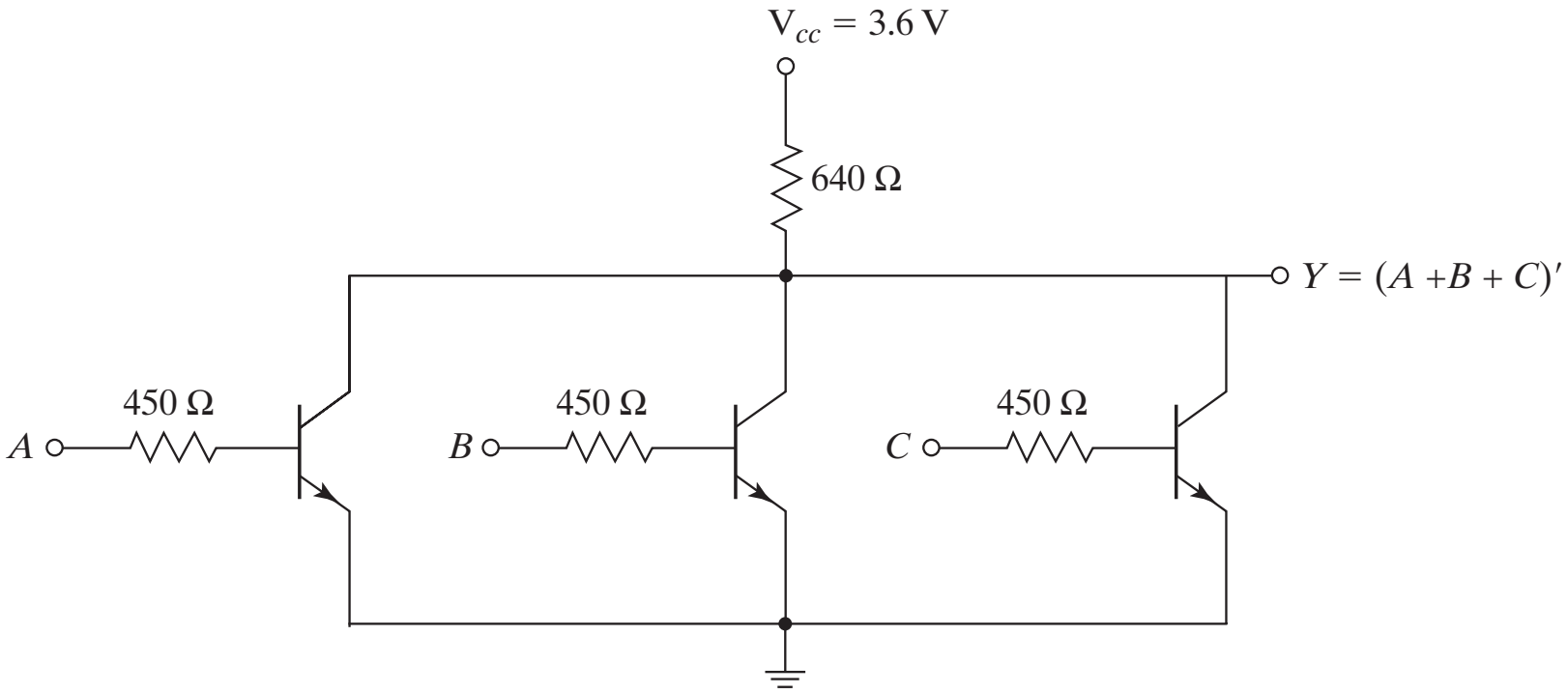


Fig. 10-8 RTL Basic NOR Gate

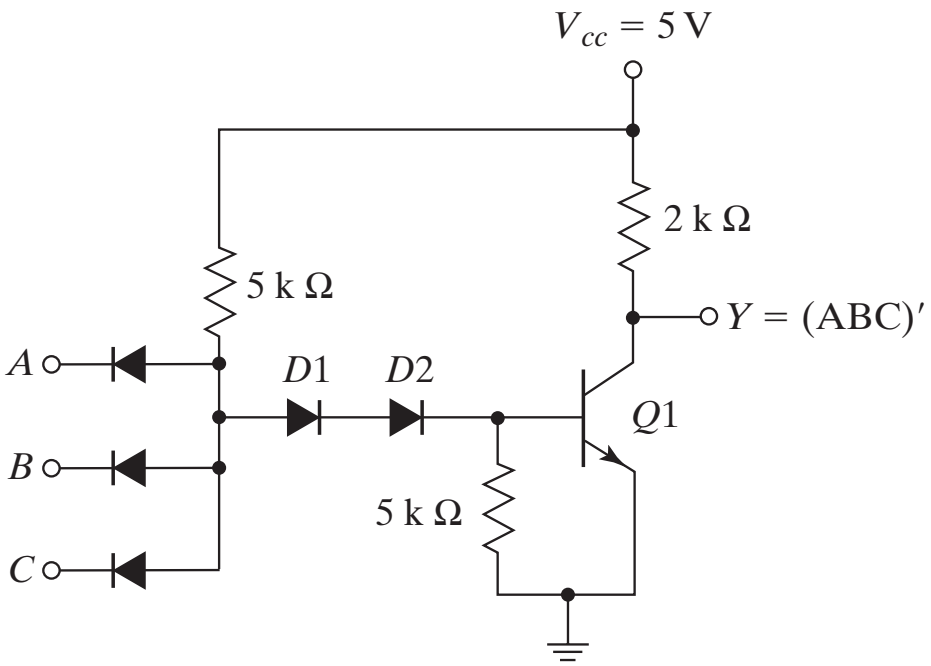


Fig. 10-9 DTL Basic NAND Gate

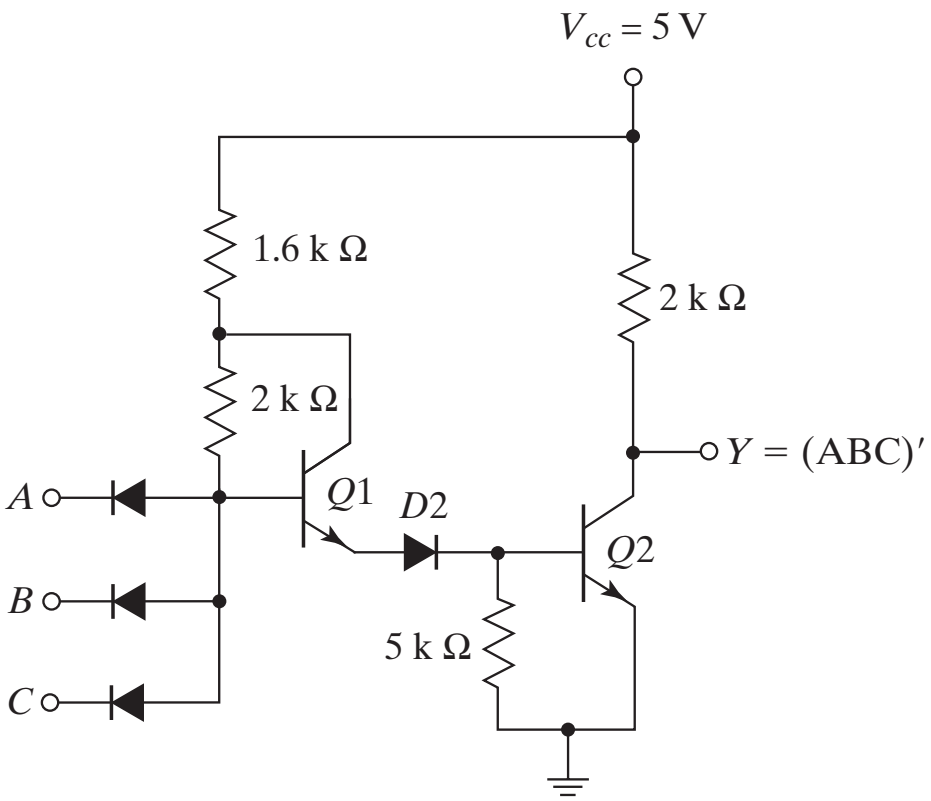


Fig. 10-10 Modified DTL Gate

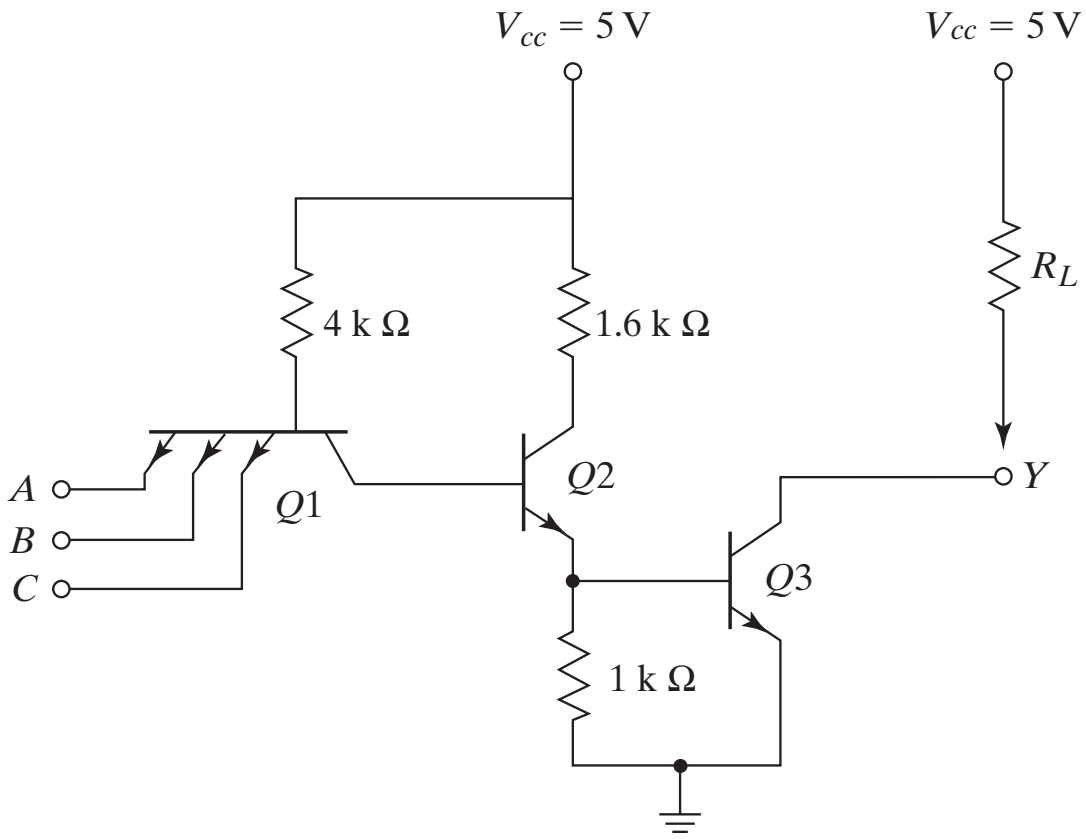
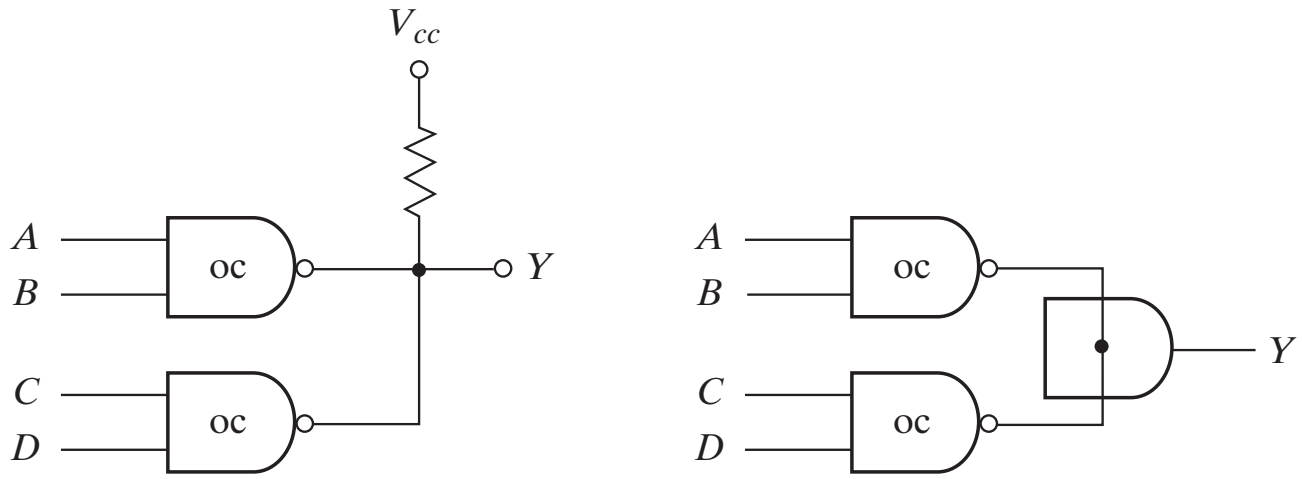


Fig. 10-11 Open-Collector TTL Gate



(a) Physical connection (b) Wired-logic graphic symbol

Fig. 10-12 Wired-AND of two Open-Collector (oc) Gates, $Y = (AB + CD)'$

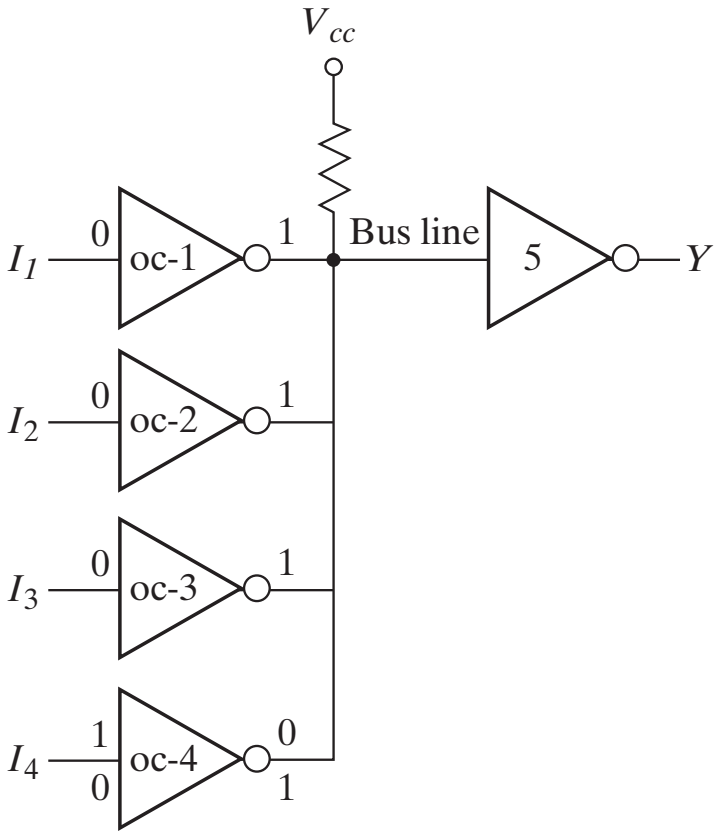


Fig. 10-13 Open-Collector Gates Forming a Common Bus Line

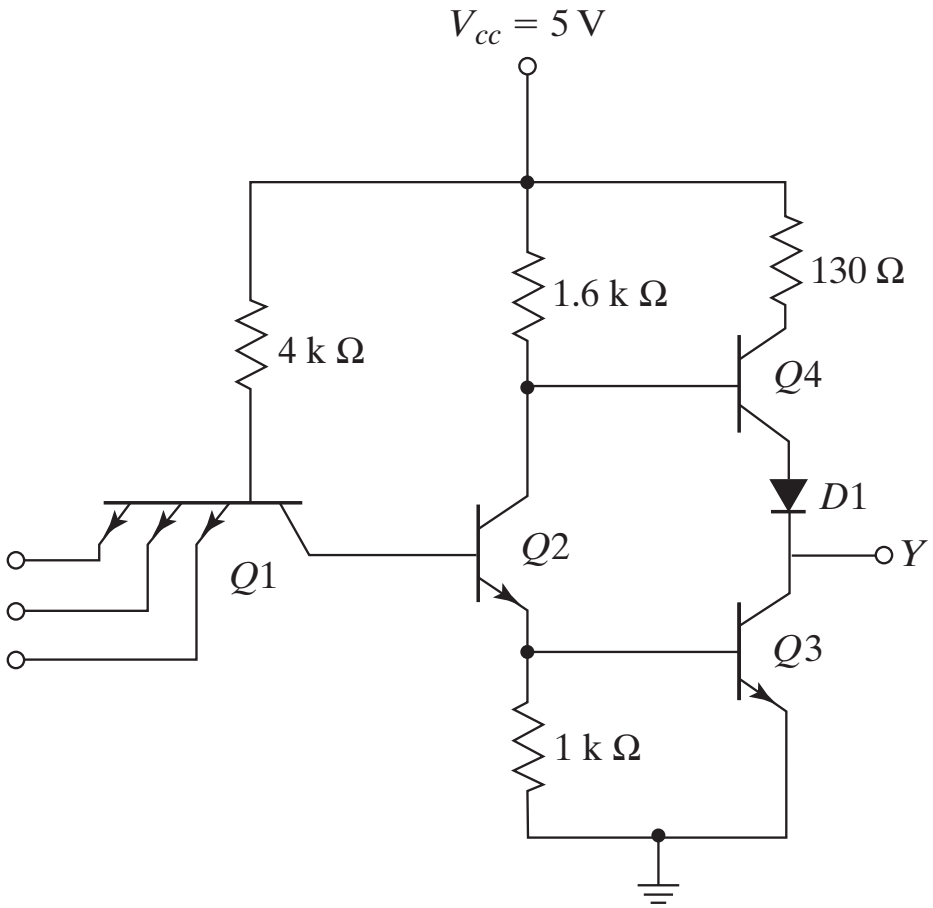


Fig. 10-14 TTL Gate with Totem-Pole Output

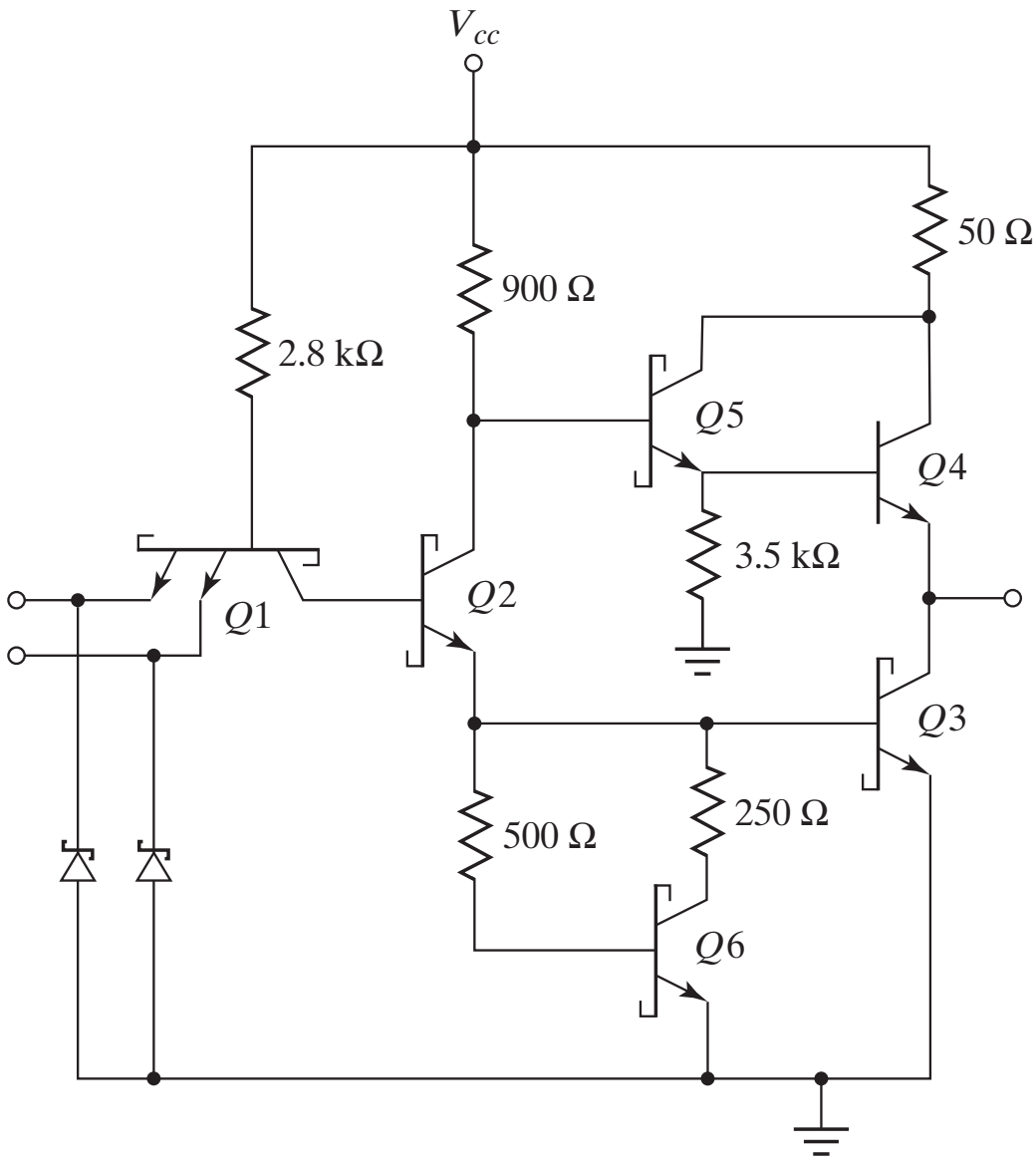
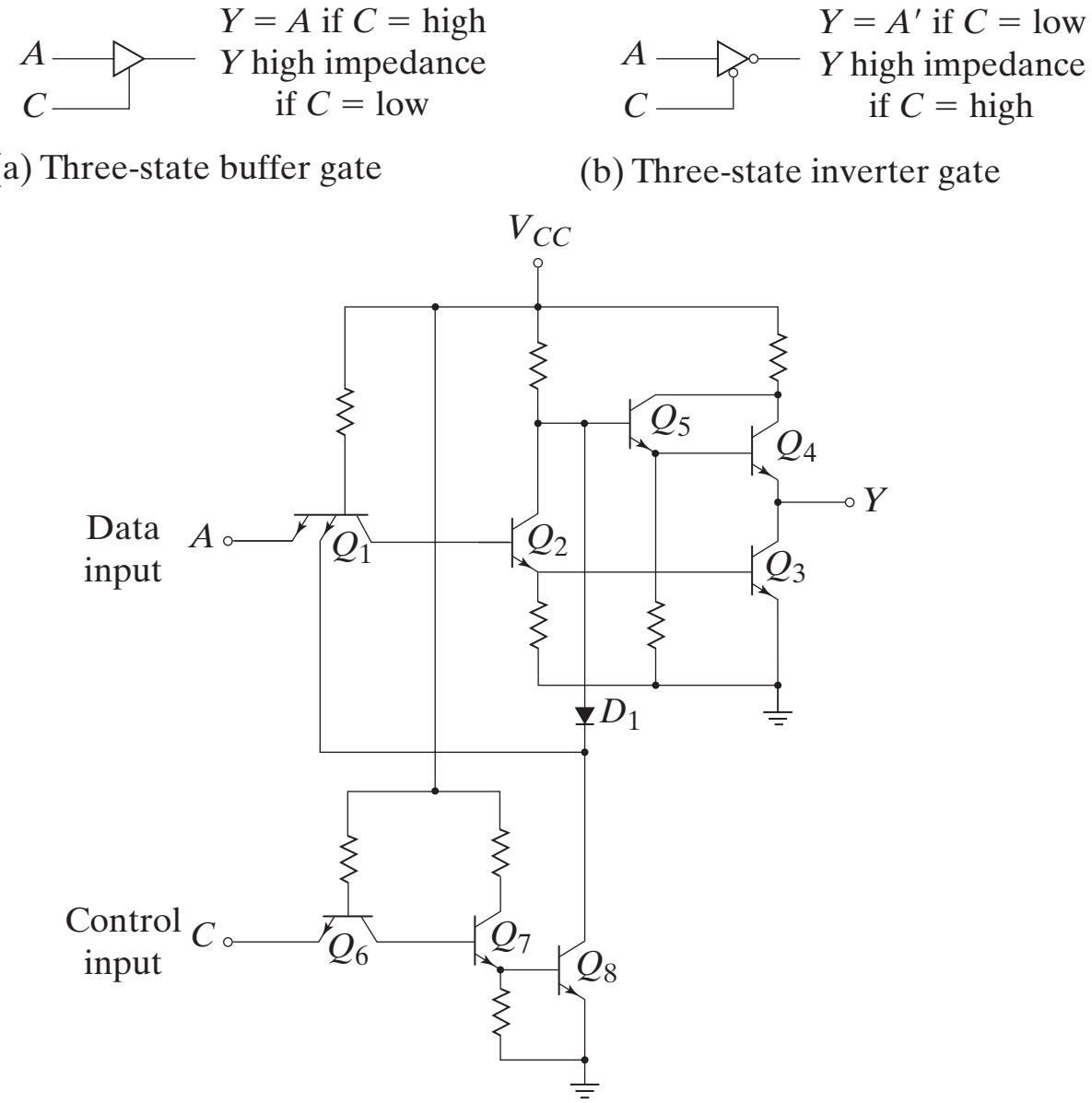


Fig. 10-15 Schottky TTL Gate



(a) Three-state buffer gate

(b) Three-state inverter gate

(c) Circuit diagram for the three-state inverter of (b)

Fig. 10-16 Three-State TTL Gate

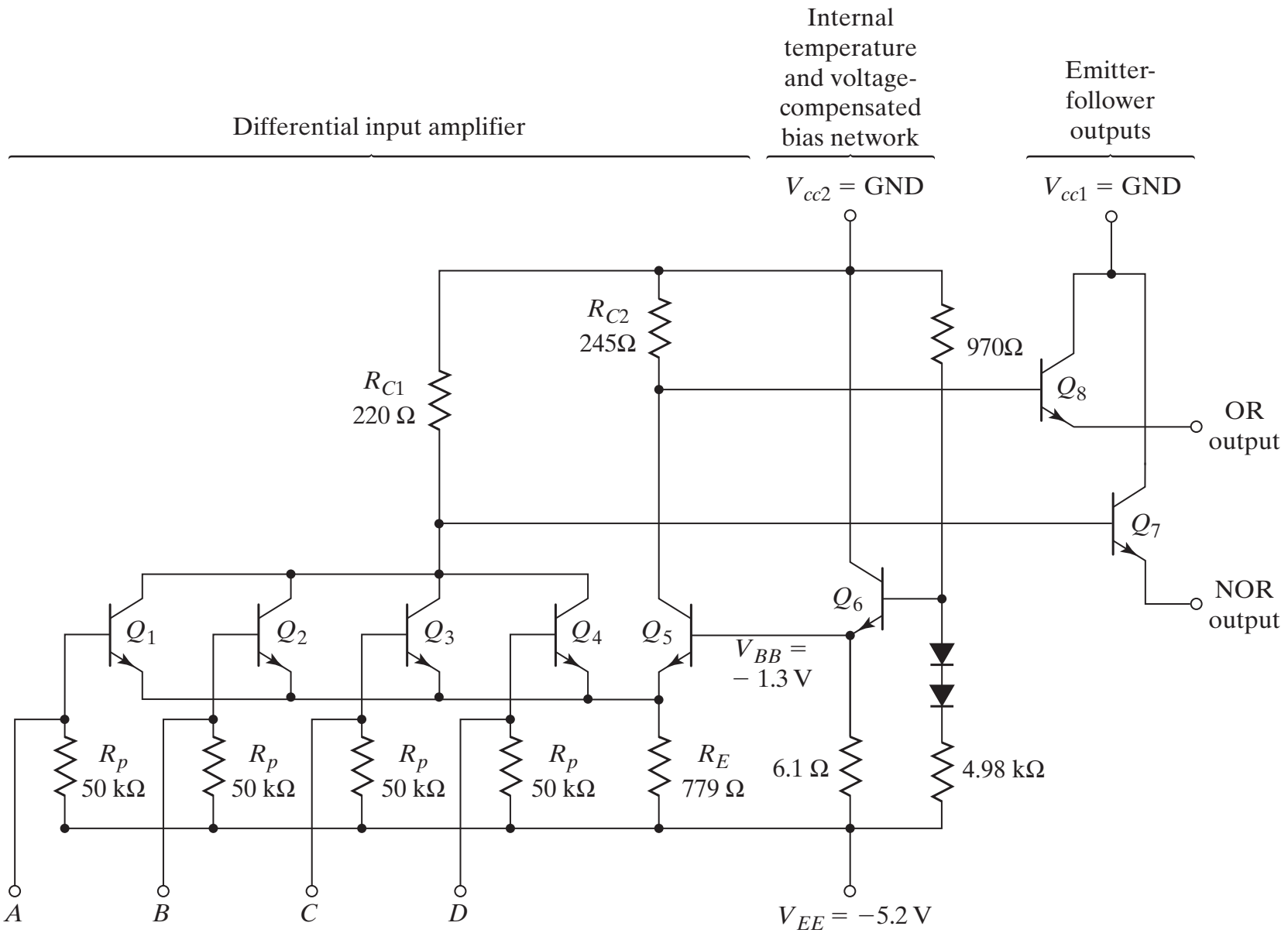
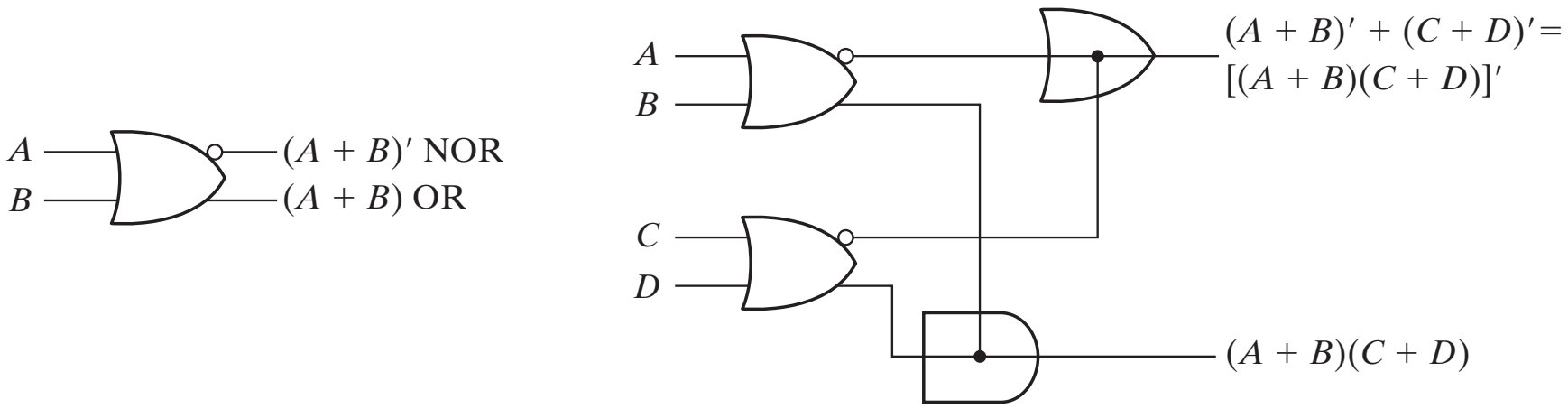


Fig. 10-17 ECL Basic Gate

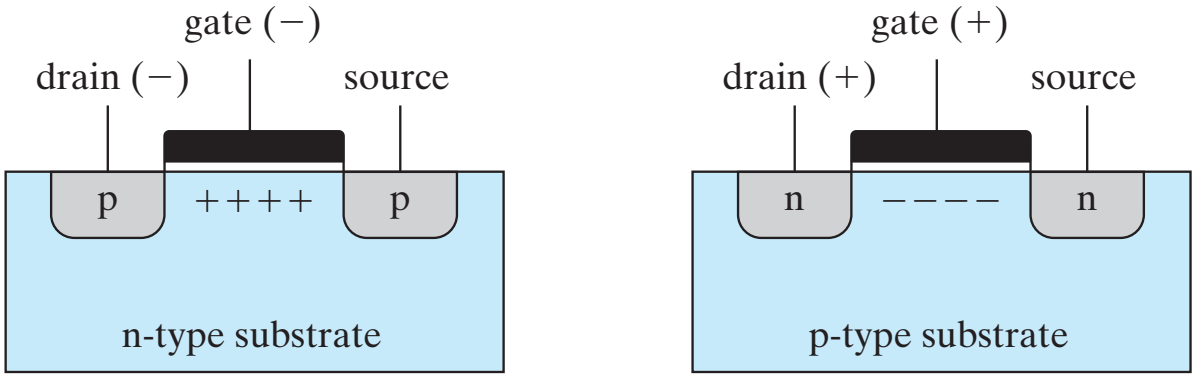
M. Morris Mano
DIGITAL DESIGN, 3e.



(a) Single gate

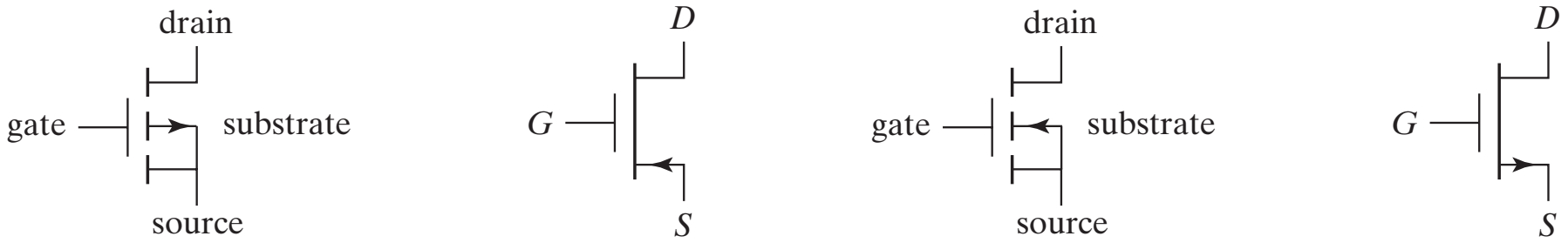
(b) Wired combination of two gates

Fig. 10-18 Graphic Symbols of ECL Gates



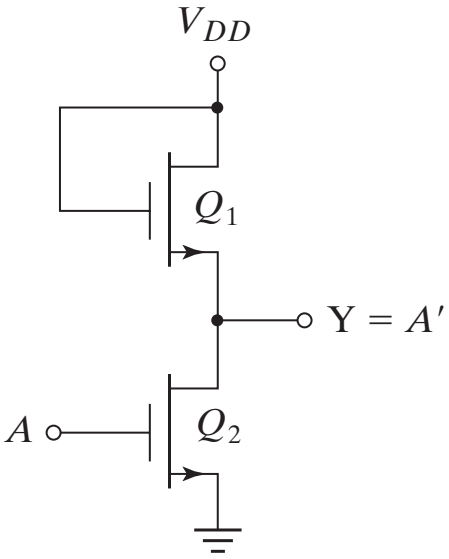
(a) p-channel (b) n-channel

Fig. 10-19 Basic Structure of MOS Transistor

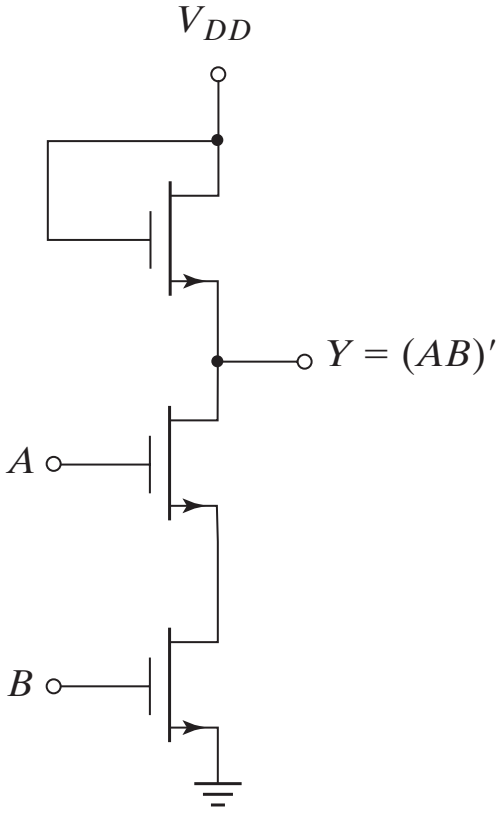


(a) p-channel (b) n-channel

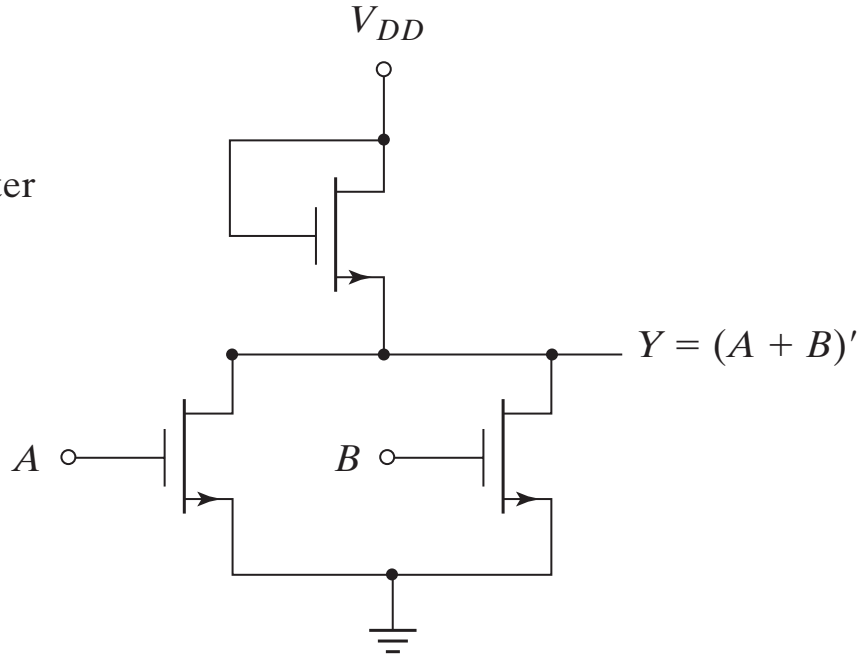
Fig. 10-20 Symbols for MOS Transistors



(a) Inverter



(b) NAND gate



(c) NOR gate

Fig. 10-21 n-channel MOS Logic Circuits

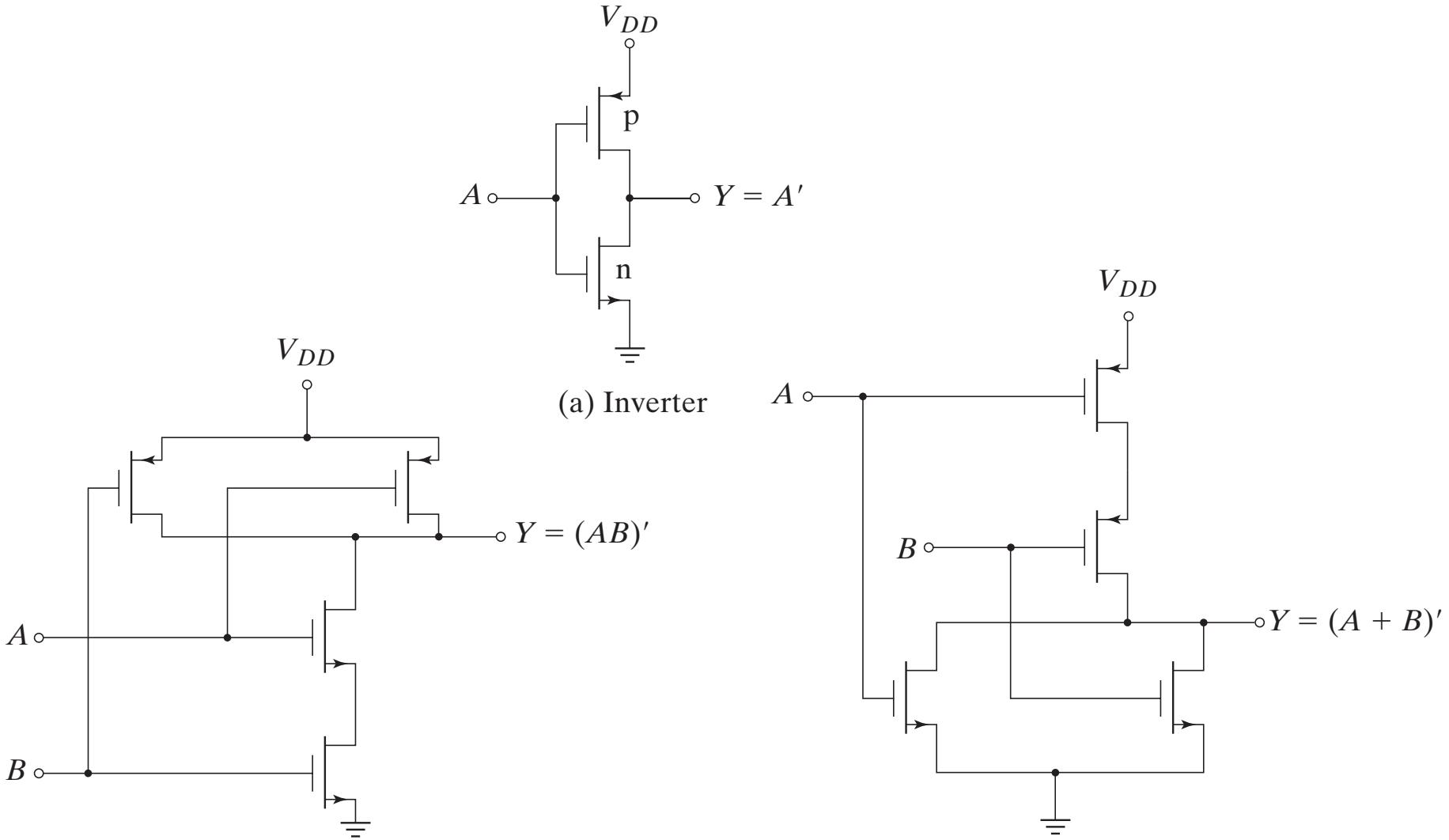
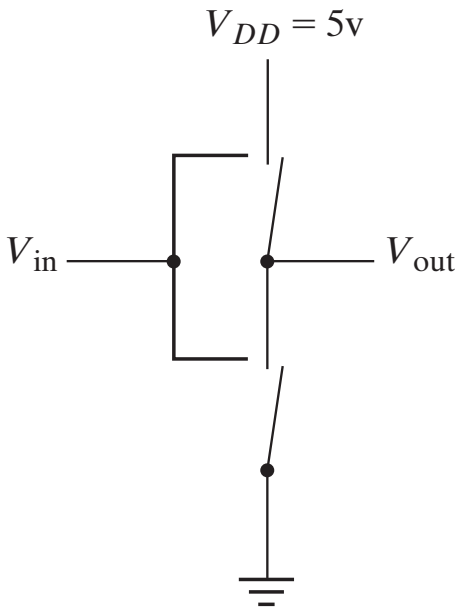
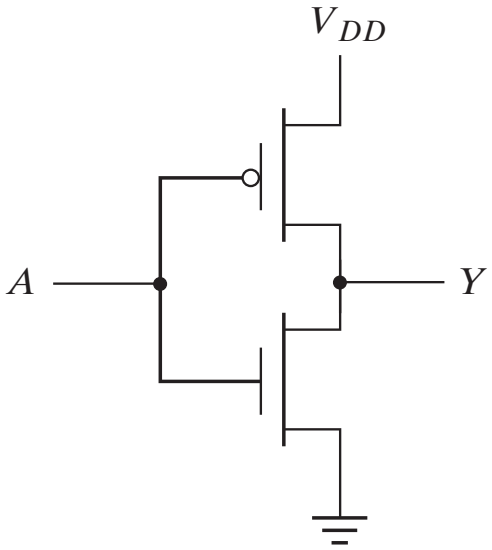


Fig. 10-22 CMOS Logic Circuits



(a) Switch model



(b) Logical model

Fig. 10-23 *CMOS* inverter

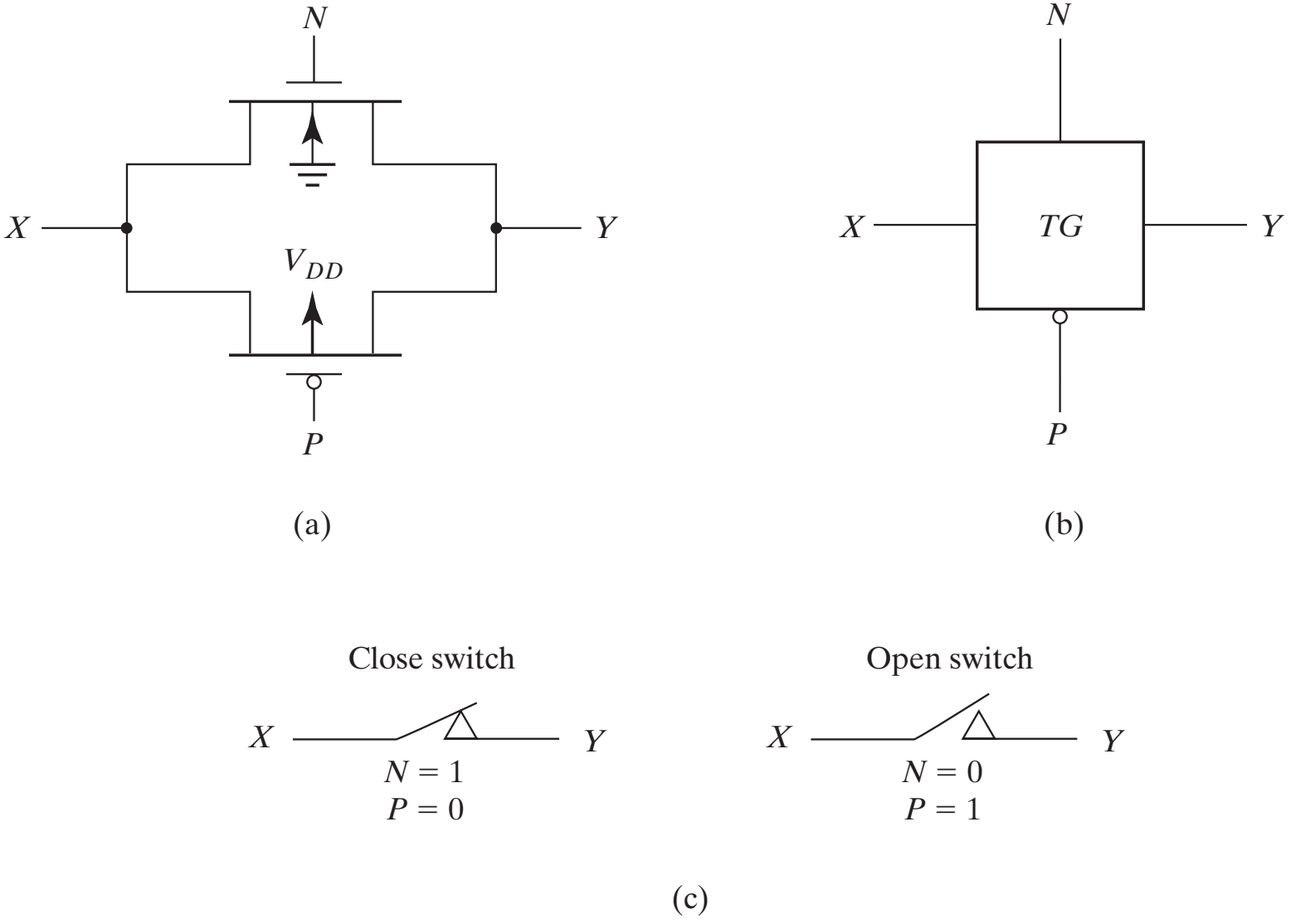


Fig. 10-24 Transmission Gate (TG)

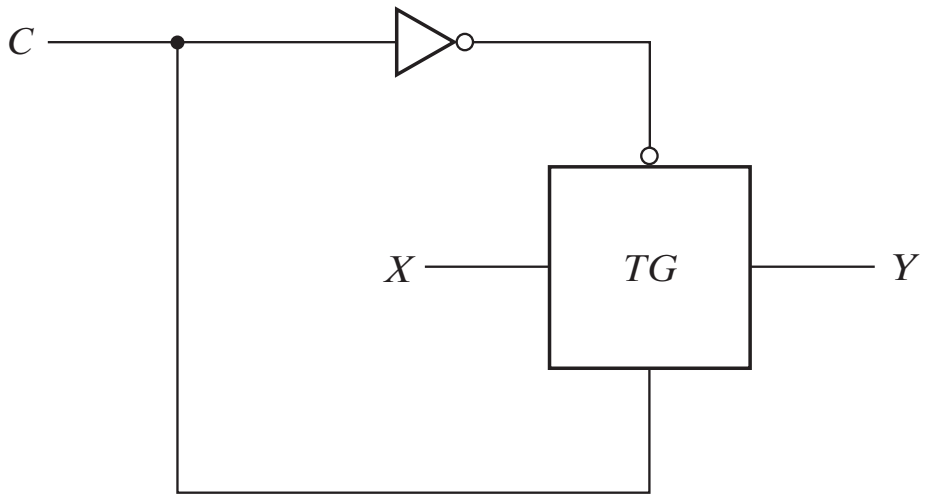
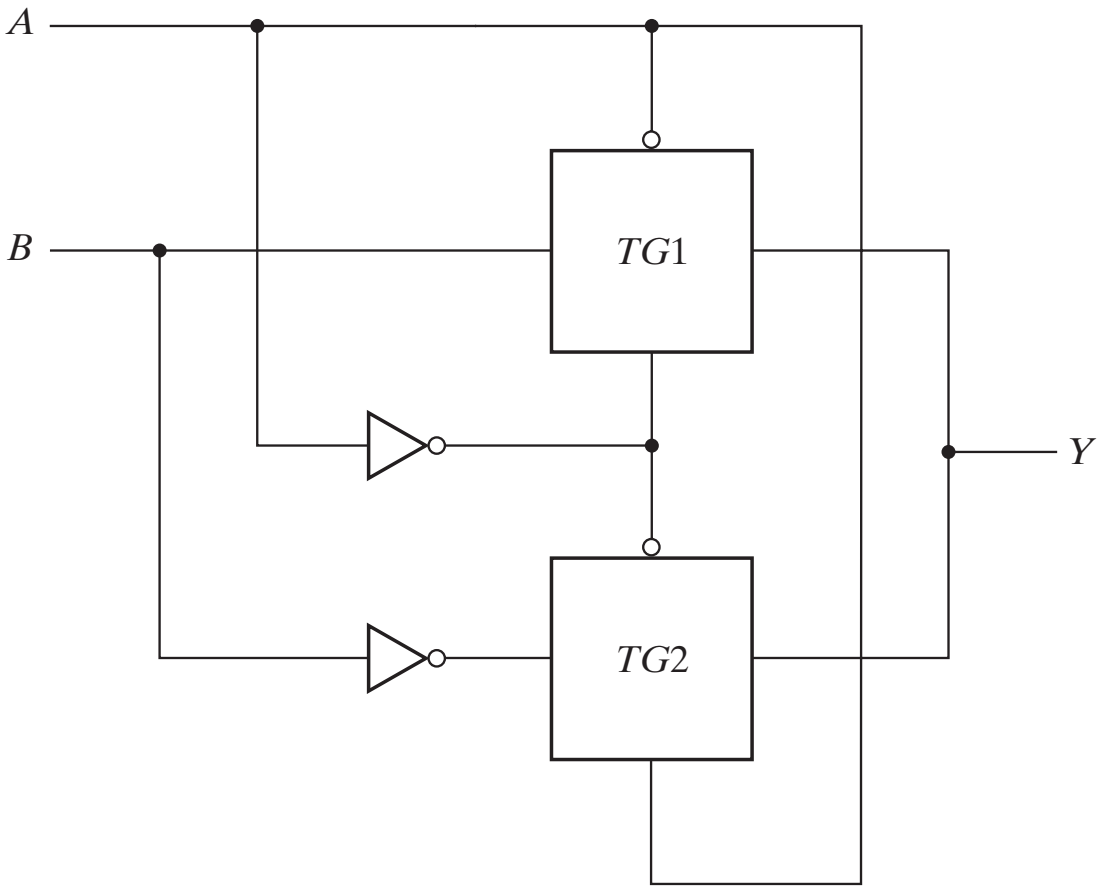


Fig. 10-25 Bilateral Switch



A	*B*	*TG*1	*TG*2	*Y*
0	0	close	open	0
0	1	close	open	1
1	0	open	close	1
1	1	open	close	0

Fig. 10-26 Exclusive-OR Constructed with Transmission Gates

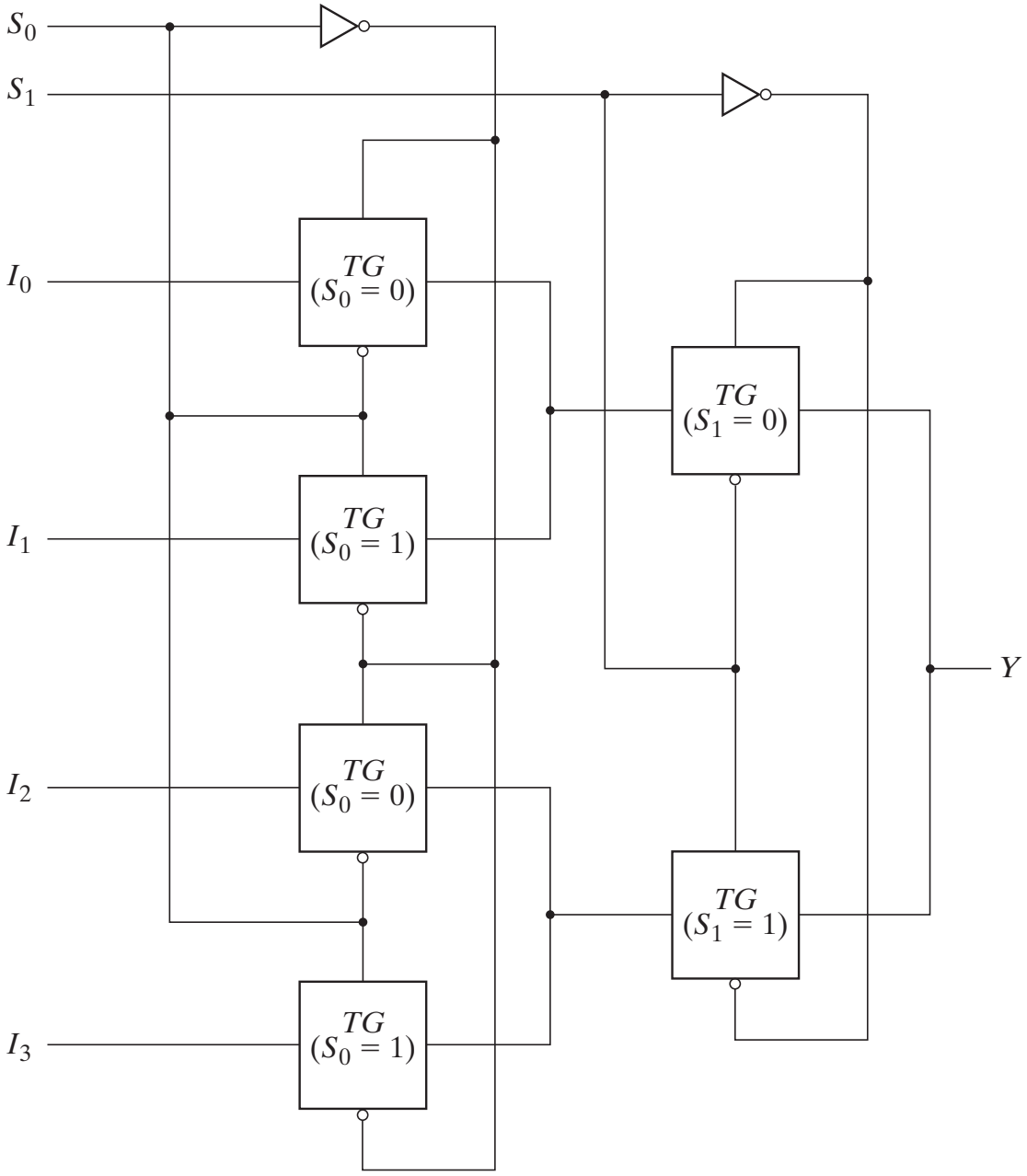


Fig. 10-27 Multiplexer with Transmission Gates

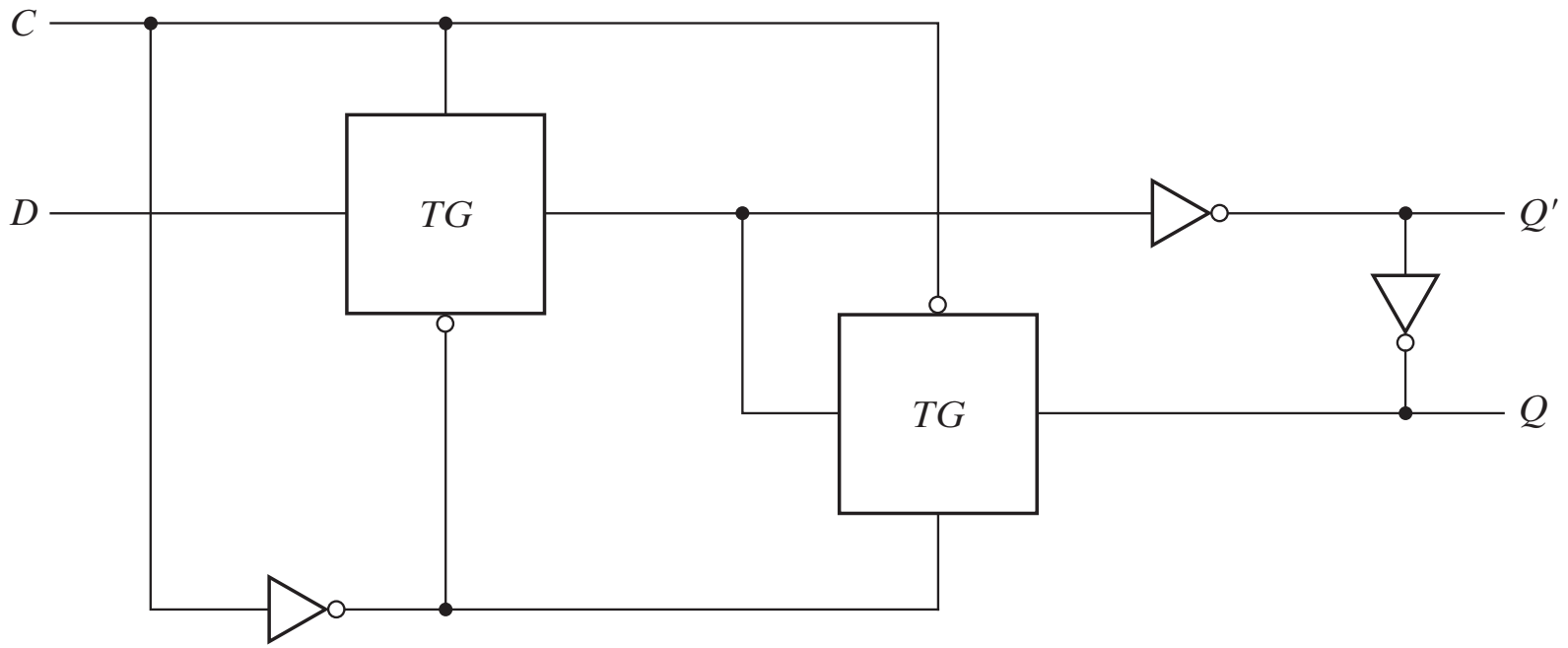


Fig. 10-28 Gated *D* Latch with Transmission Gates